

IN THE SPECIFICATION:

Page 1, before line 1, please insert the following new heading and paragraph:

Cross-Reference to Related Applications

This Application claims benefit of International Patent Application No. PCT/KR03/00051, filed January 10, 2003, which claims benefit of U.S. Provisional Patent Application No. 60/346,897, filed January 11, 2002, both of these documents being incorporated herein by reference in their entireties.

Page 3, line 10, change the header as follows:

[[Disclosure of Invention]] Summary.

Page 4, line 22, change the header as follows:

[[Best Mode For Carrying Out the Invention]] Detailed Description.

Please amend the paragraph at page 5, line 24 to page 6, line 4 as follows:

Upon charge sharing, a voltage change ΔV occurs on the corresponding bitline. Because the charge stored in the cell capacitor is very small (a capacitance of cell capacitor C may be less than one hundred femtofarads), detection of the stored voltage level usually requires amplification of ΔV . FIGURE 4 shows a schematic diagram for a sense amplifier 120a suitable for use in a device as shown in FIGURE 2. Sense amplifier 120a includes two P-channel FETs S1, S3 having their series-connected source-drain circuits connected across bitlines BL1, BL2 and their junction connected to an active-high enable signal SA-P. Sense amplifier 120a also includes two N-channel FETs S2, S4 having their series-connected source-drain circuits connected across bitlines BL1, BL2 and their junction connected to an active-low enable signal

SA-N. The gates of the pair of FETs that are connected to each bitline are connected together and to the other bitline.

Please amend the paragraph at page 6, line 34 to page 7, line 7 as follows:

Upon activation of transistor M1, charge sharing occurs between cell capacitor C1 and the (precharged) inherent capacitance of bitline BL1. As cell capacitor C1 stores a high data value in this example, the charge sharing raises the voltage on bitline BL1 by ΔV as compared to the voltage Vblp on the reference bitline BL2. Sense amplifier 120 is activated by pulling enable signals SA-P and SA-N high and low, respectively, causing sense amplifier 120 to amplify the voltage levels on bitlines BL1, BL2 to Vdd and Vss, respectively.

Please amend the paragraph at page 7, lines 8-16 as follows:

FIGURE 7 shows a timing diagram of an exemplary application of a device as shown in FIGURE 2 in a case where a low data value has been stored in cell 1 of array 110. As cell capacitor C1 stores a low data value in this example, charge sharing results in a decrease of the voltage on bitline BL1 by ΔV as compared to the voltage Vblp on the reference bitline BL2. Upon activation, sense amplifier 120 amplifies the voltage levels on bitlines BL1, BL2 to Vss and Vdd, respectively.

Please amend the paragraph at page 7, lines 17-23 as follows:

As the charge level on a cell capacitor deteriorates, the voltage change ΔV produced on the bitline upon charge sharing decreases. If the voltage change ΔV falls below the sense margin of sense amplifier 120, then the charge level can no longer be distinguished (i.e. is no longer readable by the sense amplifier), and the stored data value is lost.

Please amend the paragraph at page 9, lines 2-15 as follows:

FIGURE 9 shows a timing diagram of a device as shown in FIGURE 8 in a case where a high data value is read from a cell on bitline BL1. After the precharges on the bitlines have been equalized, and before the sense amplifier is enabled, the bias signal corresponding to the reference bitline (here, bias signal B2 corresponding to bitline BL2) is pulled low. As a result,

the voltage on bitline BL2 drops below V_{blp} by an amount ΔV_{BIAS} , and the voltage difference between the bitlines is increased from ΔV to ΔV_H (where $\Delta V_H = \Delta V + \Delta V_{BIAS}$). Although FIGURE 9 shows that bias signal B2 is pulled low after activation of wordline WL, in another implementation bias signal B2 may be pulled low before and/or during activation of wordline WL.

Please amend the paragraph at page 9, lines 16-30 as follows:

FIGURE 10 shows a timing diagram of a device as shown in FIGURE 8 in a case where a low data value is read from a cell on bitline BL1. In this case as well, after the precharges on the bitlines have been equalized, and before the sense amplifier is enabled, the bias signal corresponding to the reference bitline (here, bias signal B2 corresponding to bitline BL2) is pulled low. As a result, the voltage on bitline BL2 drops below V_{blp} by a voltage change ΔV_{BIAS} , and the voltage difference between the bitlines is reduced from ΔV to ΔV_L (where $\Delta V_L = \Delta V - \Delta V_{BIAS}$). As noted above, in another implementation bias signal B2 may be pulled low before and/or during activation of wordline WL. It may be desirable to choose a magnitude of ΔV_{BIAS} such that the voltage difference ΔV_L will not fall below a sense margin of the sense amplifier.